

### REMARKS

Claims 1-6 have been cancelled. Claims 7-11 are newly added.

The Examiner rejected claims 1 and 2 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,304,203 to Yamada, hereinafter Yamada. On the other hand, the Examiner has determined that dependent claims 3 and 4 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Taking into consideration the above observation by the Examiner, Applicant presents a set of new claims 7-11 through this Amendment. The new independent claim 7, which corresponds to original claim 1, incorporates original claim 3 and reads as follows:

A sequential comparison type AD converter comprising:  
series resistors for generating at respective connection portions reference values to convert an analog value to an m-bit digital value;  
a comparator for sequentially comparing the analog value and one of the reference values and outputting a digital value;  
a plurality of capacitive elements for distributing any one of the reference values by a capacitance ratio, **the plurality of capacitive elements including a first capacitive element and a second capacitive element**; and  
a control unit for switching a value compared to the analog value by the comparator from the reference value to a distribution value of the plurality of capacitive elements when the comparator outputs an m-bit digital value,  
wherein the analog value is converted to an (m + n) bit digital value,  
**wherein the first capacitive element and second capacitive element are connected in series between any one of the reference values and a ground, and**  
  
**wherein connection portions of the first capacitive element and second capacitive element are connected to inputs of the comparator to which the analog value is not input.**

As the Examiner admits by allowance of claim 3, the limitations in claim 7 introduced from original claim 3, i.e.,

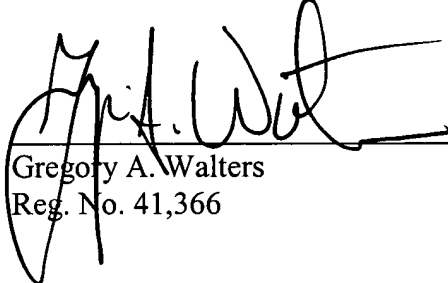
- the plurality of capacitive elements includes a first capacitive element and a second capacitive element;
- the first capacitive element and second capacitive element are connected in series between any one of the reference values and a ground; and
- connection portions of the first capacitive element and second capacitive element are connected to inputs of the comparator to which the analog value is not input; are not disclosed in the cited reference, Yamada.

Thus, Applicant respectfully submits that new claims 7-11 are not anticipated by Yamada and request that the Examiner withdraw the rejection under 35 U.S.C. 102(b).

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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